UW report: GPS time synch system update

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GPS System Block Diagram (same at both sites)

SK: { Serial TRG + Event Number
       }{ Spill Number
            Spill Trigger(s)
       }

T2K: { Spill Number

TrueTime XL-DC GPS Rcvr.

iLotus M12M GPS Rcvr.

SRS FS725 Rubidium Freq. Std.

Local Time Clock with Event Counter + Fifo

Serial I/O or optical fiber receiver

Optical Fiber Output Conv.

Required at JPARC only, for UK data system
Not included in our budget! Cost about 1K$

All parts shown are supplied by UW

SBS 616 VME-PCI

VME Bus

Linux PC

Ethernet

Optical fibers to ND280

To DAQ System
Custom VME Module (UW made):
Local Time Clock Board

- Generates timestamps from triggers + GPS data

- VME 6U
  - 100 MHz 48-bit Clock Counter
    - 10 ns least count
    - ~32 days before rollover
  - 4K x 96-bit Event Fifo Buffer
  - Optional 512x32-bit SRAM
  - 5 Trigger Inputs:
    - 2x Spill / Event Trigger
    - 2x 1PPS GPS
    - 1x Reference/CAL (Ru. 1PPS)
  - 16-bit Spill Number Output (T2K)
  - Serial TRG/Event Number Input (for SK new electronics/TRG)
  - Xilinx FPGA based (Spartan-3)
    - Adaptable as needed
  - 8-bit status input flags
  - 8 programmable AUX/CAL outputs
    - For calibration & monitoring
Local Time Clock (V7.0) prototype module

- I/O add-on board:
  - iLotus M12M GPS receiver
  - VME address select
  - Voltage regulators (+3.3, +2.5, +1.2, -5.2V)
  - Xilinx Spartan-3 FPGA
  - SRAM buffer 512x32-bit

- Spill number output (16-bit dECL)
- Serial TRG & Event# Input
- AUX outputs 6x dECL & 2x NIM
- Status inputs 8x dECL

Input/output signals of the GPS system

**Inputs:**
- 2 GPS Antenna coax cables
  - for primary and secondary GPS receivers
- (Spill) Trigger at JPARC: NIM or TTL \(\text{(decide later: easy to implement)}\)
- Secondary Trigger [optional]: NIM or TTL \(\text{ (ditto) }\)
- TRG / Event Number at Super-K: LVDS, serial format

**Outputs:**
- 1PPS (One Pulse Per Second): NIM / TTL / optical fiber
  - time marker, synchronized with UTC second increment
- Reference Clock: NIM / TTL / optical fiber for UK hardware
  - 60 MHz at Super-K
  - 100 MHz at T2K-280m \(\text{(time base = 10 MHz Ru clock)}\)
- Delayed Trigger: NIM / optical fiber
- Spill Number: 16-bit dECL (parallel) / optical fiber (serial)
  - Incremented after each spill trigger
    \(\text{(optical serial format being arranged with UK ND280m group)}\)
- Ethernet: GPS DAQ data \(\text{(method & formats to be discussed)}\)
  - LTC counts at trigger and last 1PPS edge
  - GPS quality/housekeeping data
  \(\text{(decide now...or soon? Also easy to implement)}\)
System plans

- Duplicate systems at JPARC and SK
  - primary + secondary receivers and antennae
  - LTC board + Rubidium clock
  - VME crate with Linux workstation controller and UPS
- Complete duplicate backup set of parts at each site
  - 2 of everything on site, at both ends of neutrino beam
  - Decision: spare parts cold, or hot?
    - Run “spares” also?
      - Could station spares in another building, and run at all times (data to archive logfiles only)
        » Hot backup, remotely switchable into T2K datastream immediately in case of power failure or earthquake damage to original online hardware
- Or, cold backup: leave them in storage (no burn time, brand new if/when needed)
  - Hans comments: probably hot is better: SK system has run for 10 years with no failures! eg, Ru oscillator has MTBF = 20 years...
GPS To Do List

- **FPGA code development for LTC**
  - very similar for both GPS and ADC boards needed for T2K
  - Concentrated on ADC board development first, since it is new
  - New LTC board prototype v. .0 now ready

- **Finalize design of optical fiber interface modules**
  - For Super-K: optical receiver for GPS signals from Radon Hut
    - IRIG-B data, 1PPS (1Hz) sync, slow serial data
  - For T2K: optical transmitter for GPS signals to ND280 DAQ
    - 100 MHz, 1PPS (1 Hz), spill number, spill trigger

- **GPS system integration & testing**
  - Now using old-model rack receivers recovered from K2K
  - Test and iterate prototype LTC design (if needed)
  - Target finalization date: 9/30/2007 (this means: still tweaking but within \( \varepsilon \) of ready to ship)
    - Test and debug onboard and online software

- **Final purchases /construction**
  - Can wait for funds: postponable to (say) mid '08?
  - Make and test full set of LTC modules (2 for each site): allow 2 months
  - Purchase remaining off-the-shelf commercial items for full GPS system
UW Task Plans/Timelines

- **GPS time synch system**
  - Finalize conceptual design: Done
  - Finalize schematics & layout designs: Done
  - LTC prototype construction: Done
  - Finalize FPGA logic: 9/07~10/07
  - LTC prototype system integration and testing: 9/07~10/07
  - Optical fiber module design & prototyping: 9/07~11/07
  - Board production: 12/07~3/08
  - Order commercial units (when US funds available): 4/08(?)
  - Integrate and test system in Seattle: 4/08~6/08
  - Ship to Japan and install at JPARC and SK: 7/08~12/08