TFB electronics workshop

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Front-end Electronics

- UK groups sent TFB and RMM boards to set up three test systems in the US for general electronics (Pitt) and photo-sensor testing (CSU, LSU).
Workshop

- Purpose: set up and test all three test systems at Pitt and demonstrate basic operation/functionality of the TFB electronics

- Held last week (Nov. 5-8) at University of Pittsburgh

- Participants:
  - UK (RAL and IC):
    - Matt Noy (TFB)
    - Tobi Raufer (software)
    - Mohammed Siyad (RMM)
    - Matt Thorpe (DAQ)
  - US:
    - Dmitriy Beznosko (SUNY-SB)
    - Yvan Caffari (CSU)
    - Brandon Hartfiel (LSU)
    - D. Naples (Pitt)
    - V. Paolone (Pitt)
    - I. Danko (Pitt)

Many thanks!

also stopped by

- D. Warner (CSU)
- R. Wilson (CSU)
Initial setup

- TFB and RMM worked fine
  - firmware update is possible in the future – e.g. to resolve problem with buffer overflow in RMM (right now it requires very fast PC to read out data from RMM without hanging the RMM)

- Control PC:
  - Scientific Linux 4.4/4.5
  - Gigabit/Ethernet server adapter (Intel PRO/1000 MF) to communicate with RMM via optical link

- CSU and LSU has brought (sent) their own computer for the workshop so that each institution could take home its own tested system
  - initial problem with Pitt computers: firewall setting prevented data transfer from RMM (optical card had to be explicitly set as a trusted port)
• Typical DAQ sequence:
  - PC requests an event from RMM
  - RMM sends trigger to TFB
  - TFB takes care of
    - generates synchronous external trigger (only for test purposes)
    - Trip-t operation (integration/reset cycles)
    - sequencing Tript-t pipeline readout and digitization
    - formatting and transmitting data back to RMM
  - RMM transmits data to PC

Trip-t integration and reset cycles:
• 23 periods
• programmable in 10ns increments

TFB external trigger:
• 160 ns wide
• first integration period starts about 200ns after rising edge
Software

- **DAQ:**
  - controlled via a simple menu
  - basic TFB parameters can be set/checked (integration/reset time, HV trim etc.)
  - set up calibration run using on-board charge injection (single or multiple injection)
- **Data is written to binary file**
  - ADC values from all 64 channels (high/low gain) and 23 integration cycle
  - Additional info (e.g. temperature of board etc.)
- A standalone C++ program converts the binary output to a ROOT tree
Calibration run

- Simple test of functionality using on-board charge injection circuitry
  - internal test pulse coupled through 10 pF capacitor to groups of 4 input channels
  - test pulse can be set in units of 5V/4096 (≈1.22 mV)
  - single injection or multiple injection using equidistant voltage steps

Multiple injection: from 100-900 in steps of 100 (in unit of 1.22 mV)
External charge injection

- Tested external charge injection by driving a pulse generator using the TFB's external trigger signal
  - TFB trigger is brought out as an LVDS signal pair – requires special circuitry to convert signal to single ended standard TTL signal compatible with pulse generator input
  - Pulse generator input has to be capacitively coupled to TFB input
- We used Matt Noy's components (converter and cables) during the test
Test with SiPM

- Using one of the SiPMs brought by Dave Warner and an LED triggered by pulse generator
Test system at Pitt
Plans at Pittsburgh

• Need some additional components:
  – we already have one LVDS-to-TTL converter board for external triggering (will send a 2\textsuperscript{nd} board to CSU)
  – need to modify miniature coax cables to use for external charge injection

• Near term plan
  – do some initial linearity tests using the on-board charge injection
  – using external charge injection:
    • test two different cable diameter 1.13 mm (single shielded) and 1.32 mm (double shielded)
    • test different cable lengths – available up to 2m but currently we have only 1 m cables