GPS time synchronization system for T2K

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T2K GPS Time Synchronization: overview

GPS provides time synchronization accurate to O(10) nanoseconds

Super-Kamiokande

293 km of earth

2 km intermediate detectors(?)

Kamioka


ν target, monitors

proton beam

280m detectors

JPARC proton accelerator

JPARC site
Concept

• Update GPS synch system used successfully in K2K
  - Systems at each site are identical (except for site-specific DAQ requirements)
  - Use GPS data to synchronize local clock with UTC
  - Provide multiple backups since timestamps are critical data

• For T2K:
  - Use newest models of commercial components
  - Build new versions of custom boards, adapted to T2K DAQ plans
  - Provide on-hand swap-in backups at each site, so non-expert shift physicist can replace units if needed
GPS time system design:

**Duplicate systems at JPARC and Super-K:** each site has

- 2 independent GPS receivers + antennae:
  - Laboratory-standard Symmetricom/TrueTime XL-DC
  - OEM engine (iLotus M12m)

- Rubidium Frequency Standard (SRS FS725):
  - 10 MHz → 50–100 MHz output via PLL Multiplier (for DAQ + LTC)
  - GPS synchronized with 1PPS input
  - Low-jitter 1PPS output

- UW-made Local Time Clock (LTC) board
  - Hosts Ru clock and GPS receivers, interfaces to VME

- VME modules for real-time data/signal processing:
  - TRG Event Counter (ICRR-made for Super-K)
  - Serial Data I/O module, and optical fiber interfaces for 280m DAQ

- Linux PC:
  - Link to VME modules via SBS 616 VME-PCI
  - Real-time GPS DAQ and housekeeping/QC software
  - Ethernet to/from local online DAQ system

*Also: On-site swap-in backups provided for all components*
GPS System Block Diagram (same at both sites)

SK:  
{  
  Serial TRG +  
  Event Number  
  Serial Event# in (32-bit)  
}

T2K:  
{  
  Spill Number  
  Spill Trigger(s)  
}

Local Time Clock  
with  
Event Counter  
+  
Fifo  

Serial I/O or  
optical fiber receiver  

Optical Fiber Output Conv.  

SBS 616 VME-PCI  

All parts shown are supplied by UW  

VME Bus  

Linux PC  

Ethernet  

To DAQ System  

Required at JPARC only, for UK data system.
Custom VME Module (UW made):
Local Time Clock Board

- Generates timestamps from triggers + GPS data

- double-width VME 6U board
- 100 MHz 48-bit Clock Counter
  - 10 ns least count
  - ~32 days before rollover
- 4K x 96-bit Event Fifo Buffer
- Optional 512x32-bit SRAM
- 5 Trigger Inputs:
  - 2 x Spill / Event Trigger
  - 2 x 1PPS GPS
  - 1 x Reference/CAL (Ru. 1PPS)
- 16-bit Spill Number Output (T2K)
- Serial TRG/Event Number Input (for SK new electronics/TRG)
- Xilinx FPGA based (Spartan-3)
  - Firmware adaptable as needed
- 8-bit status input flags
- 8 programmable AUX/CAL outputs
  - For calibration & monitoring
FPGA logic for LTC

We can change code (→ LTC operation and performance) as needed.
Local Time Clock (v7.0) prototype: ~ready @ UW
Components

- **Lotus M12M**
  - 12 satellites simultaneously
  - Better than 6 ns at 6-sigma

- **Stanford Research FS725 Ru oscillator**
  - Inputs for GPS 1PPS synch
  - 20 yr aging < 0.005 ppm

- **Symmetricon TrueTime XL-DC**
  - 1 PPS, IRIG B time code and serial I/O time strings
  - Frequency accuracy better than $1 \times 10^{-12}$
GPS To Do List

- **GPS system integration & testing**
  - Now using Truetime receiver recovered from K2K
  - Finalize LTC: ~ today! (Hans is still tweaking FPGA code, otherwise ready)
  - Integrate system in Seattle and test end-to-end
  - Finalize onboard and online software

- **Finalize and prototype optical fiber interfaces**
  - For Super-K site: optical receiver for GPS signals from Radon Hut
    - IRIG-B data, 1PPS (1Hz) sync, slow serial data
  - For JPARC site: optical transmitter for GPS signals to ND280 DAQ
    - 100 MHz, 1PPS (1 Hz), spill number, spill trigger

- **Full system purchases/construction**
  - Must wait for US funds to be available: ~ March ’08?
  - Make and test full set of LTC modules (2 for each site): allow 2 months
  - Purchase remaining off-the-shelf commercial items for full GPS system
UW Task Plans/Timelines

- **GPS time synch system**
  - Finalize conceptual design: Done
  - Finalize schematics & layout designs: Done
  - LTC prototype construction: Done
  - Finalize FPGA logic: ~Done
  - LTC prototype system integration and testing: Now
  - Optical fiber module design & prototyping: 10/07~11/07
  - Integrate and test prototype system: 11/07~12/07
  - Board production: 12/07~3/08
  - Order commercial units (when US funds available): 4/08
  - Integrate and test system in Seattle: 4/08~6/08
  - Ship to Japan: 7/08
  - Install and test at JPARC and SK: 7/08~12/08 (?)
  - Berns and Wilkes will do this