GPS system and monitor electronics: progress report from UW

Hans Berns and Jeff Wilkes
University of Washington, Seattle
US T2K Collaboration Meeting
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Local Time Clock (v7.0) prototype: ~ready @ UW
UW Task Plans/Timelines

• GPS time synch system
  - Finalize conceptual design Done
  - Finalize schematics & layout designs Done
  - LTC prototype construction Done
  - Finalize FPGA logic Done
  - LTC prototype system integration and testing Now
  - Optical fiber module design & prototyping Now
  - Integrate and test prototype system Now
  - Order commercial receivers Now
  - Finalize LTC firmware by 5/1
  - LTC board production begin 5/08
  - Integrate and check full systems in Seattle 5/08~6/08
  - Ship one set to Japan (Super-K) 7/1/08
  - Ship 2nd set to Japan (JPARC) 8/1/08
  - Install and test at JPARC and SK 7/08~12/08 (?
    • Berns and Wilkes will handle this
UW FADC PROTOTYPE 2: 125 MHz

- Prototype v.2 ready (shipped to KEK)
  - Designed and built at UW
  - 8 ch /board, 12bit ADC
  - Performance may be customized for T2K as required
  - >125 MHz sampling (160 OK)
  - Pulse stretcher on inputs
  - Testing completed @ UW
  - Construction under way
FADCs for beamline monitors

Timeline for custom FADC production:

1. Testing of modifications on prototype-1: Sep 07 √
2. Prototype-2 ADC board design: Oct/Nov 07 √
3. Testing and evaluation of proto-2: Feb 08 √
4. Design finalized: Now √
5. Proto 1 sent to KEK Now √
6. Construction of boards in Seattle: Apr-Jun 08

This schedule meets demands of T2K beamline monitor team.
Status summary: design finalized, ready to produce
Production of boards is straightforward: resources on hand
Parts and etched boards ordered
• Shown previously…
UW FADC Board for ESMs and CTs

- Uses FPGA to control and interface FADCs
- VME board hosts chipsets
- Status (as of Feb, 2008)
  - Proto 1 board completed and tested (3/07)
    - 80 MHz ADCs
    - Hardware and FPGA software works
    - Used at ESM beam test in Kyoto
    - 8 channels on proto, but higher density possible
  - Proto version 2: finished and tested
    - 125 MHz ADCs
      - Overclocked to 160 MHz: OK!
    - Pulse stretcher on inputs
      - Can be adjusted during beam commissioning: does not affect board layout

ADC card block diagram MGB 4/2007
125 and 160 MHz sampling tests

Results exceed expectation!
Design finalized